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AMENDMENT TO THE SPECIFICATION

Please replace the paragraph beginning on page 28, line 4 to page 29, line 4 with the following:

Combined Y-code estimate: In a further embodiment of the present invention, the primary accumulator 82 operates functionally as an adder which adds a sequence of despread (with a locally generated replica of the P-code) samples over one W-code interval signaled by *WchipEdge*. The secondary accumulator 84 operates as a combiner which combines the primary values of the primary accumulator 82 and the estimated W-code chip. One method of combining includes summing the values output by the primary accumulator 82 multiplied by the estimated W-code chip value. However, the present invention includes other methods of combining. For instance, the present invention includes combining the outputs of the primary accumulator 82 in dependence upon a confidence level in each output from accumulator 82. The estimated W-code chip is obtained by comparing the absolute values of the primary accumulator of the Q-branch of the complex primary accumulator value of the first integrator 82 of the L1 and L2 channel. The estimated W-code chip value (or Y-code value) is the sign bit of the largest value from this comparison. Because of the lower transmit power, a scaling value may be applied to the L2 signal which is usually more powerful than the L1 signal. A value of 0.75 is suitable. The secondary accumulator integration buffers 85 are updated on IntEpoch strobes. Fig. 14 shows one embodiment of the selection logic required to provide the Y-code estimate indicated above. The outputs of the primary accumulators 82L1 and 82L2 are for the L1 and L2 channels, respectively are applied to absolute value circuits 861, 862, respectively, whereas the sign of each of these primary accumulated outputs is transferred to a Y-code estimate selector (or W-cod chip estimate selector) 865. In absolute value circuits 861, 862 the absolute value of the respective primary accumulator value is determined. The absolute value output from circuit 862 may be modified to allow for received power differences between the L1 and L2 signals, e.g. it can be multiplied by a factor such as 0.75 (multiplier ~~864~~863). The modified absolute values are input to a comparator 864 which compares the two absolute values and outputs a signal to a Y-code estimate selector 865 indicating which of the signals from L1 or L2 has the largest absolute value. The selector 865 selects the sign of the signal with the largest absolute value as the value for the W-code chip or, optionally, an alternative value. The optional alternative value may be

zero, e.g. when the confidence in the result is low. The output for the Y-code estimate selector 865 is combined with each of the primary accumulated values of the L1 and L2 accumulators 82L1 and 82L2 for use in the secondary accumulators 84L1 and 84L2 respectively.